



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/936,479	09/13/2001	Siegfried Schweidler	PD990014	6074

7590 06/12/2006

Joseph S Tripoli
Thomson Multimedia Licensing
PO Box 5312
Princeton, NJ 08540

EXAMINER

LI, ZHUO H

ART UNIT	PAPER NUMBER
----------	--------------

2185

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicant(s)

09/936,479

Applicant(s)

SCHWEIDLER ET AL.

Examiner

Zhuo H. Li

Art Unit

2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 and 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Boyer et al. (US PAT. 5,410,546 hereinafter Boyer).

Regarding claim 1, Boyer discloses a method for management of data received via a serial data bus (108, figure 1), in a receiving device (107, figure 1) comprising the steps of receiving data packet transmitted in bus packets having a variable length (col. 6 lines 12-15), each bus packet having a header portion of the packet, read as a header, and a data portion, read as a payload data field, the data portion being divided into data blocks having a defined length, i.e., to write the variable length data packet into page buffers having a defined length (col. 20-24 and col. 10 lines 31-35), a combination of a defined number n of data blocks forming a data source packet of fixed length, i.e., combining a defined number of multiple page buffers forming a data packet of fixed length (col. 6 lines 26-40 and col. 10 lines 9-17), section-by-section transmission of the data source packet within the framework of data blocks being permitted, i.e., reading data from page buffers and applying the data to the Block storage device (col. 10 lines 35-64), and a counter (415, figure 4) for carrying out a modulo- n counting of the data block in

Art Unit: 2185

order to determine the data source packet boundaries (col. 13 lines 1-23) and in that the beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval (col. 13 lines 30-64 and col. 16 line 66 through col. 17 line 6).

Regarding claims 2-3, Boyer discloses each bus packet being subject to CRC checking and the checking results being buffer-stored in order to be able to ascertain whether a data source packet transmitted in two or more bus packets has been transmitted without transmission errors, wherein a reference count reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data block is effected and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal is output in the event of non-correspondence (col. 7 lines 11-24).

Regarding claim 5, Apparatus for managing data received data via a serial data bus (108, figure 1) in a receiving device (107, figure 1) comprising a receiver for receiving data transmitted in bus packets having variable length (col. 6 lines 12-15), the bus packet having a header portion of the packet, read as a header, and a data portion, read as a payload data field, the data portion being divided into data blocks having a defined length, i.e., to write the variable length data packet into page buffers having a defined length (col. 20-24 and col. 10 lines 31-35), a combination of a defined number n of data blocks forming a data source packet of fixed length, i.e., combining a defined number of multiple page buffers forming a data packet of fixed length (col. 6 lines 26-40 and col. 10 lines 9-17), section-by-section transmission of the data source packet within the framework of data blocks being permitted, i.e., reading data from page buffers

Art Unit: 2185

and applying the data to the Block storage device (col. 10 lines 35-64), having a memory unit, i.e., data array (410, figure 4), to which received data are written in order and having a memory management device (411, figure 4) when a modulo-n counter (415, figure 4) is provided, which counts the received data blocks and outputs a data source packet start signal to the memory management device at the beginning of the next counting interval (col. 13 lines 30-64 and col. 16 line 66 through col. 17 line 6).

Regarding claims 6-7, the limitations of the claims are rejected as the same reasons as set forth in claims 2-3.

Regarding claim 8, Boyer discloses the counter (415, figure 4) by which data are counted in particular in units of bytes and which outputs a data block counting signal if the number of data that have been countered are as many as defined as belonging a data block (col. 13 lines 1-23).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

Art Unit: 2185

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyer et al. (US PAT. 5,410,546 hereinafter Boyer).

Regarding claim 4, Boyer differs from the claimed invention in not specifically teaching wherein the defined number n of data blocks of a data source packet corresponds to the number 8 and the modulo- n counting is correspondingly modulo-8 counting. However, it is old and notoriously well known in the art of having the defined number of n data blocks corresponding to the number of 2 to power x , where $x = 1, 2, 3, \dots$, in which 8 is equal to 2 to power 3. In addition, utilizing modulo-8 counter do not have a disclosed purpose nor overcome any deficiencies in the prior art such that the number of n of data blocks of a data source packet may contain any number, i.e., 2, 4, 8, Note Boyer teaches DRAM ARRAY being logically subdivided into equal size section (col. 10 lines 31-35) and state control logic for determining the boundaries of page buffers within DRAM ARRAY (col. 10 lines 35-40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Boyer in utilizing modulo-8 counter for counting 8 of data blocks of a data source packet, as disclosed supra, because applicant does not disclose that the number 8 and modulo-8 counting, as opposed to other size, overcome a deficiency in the prior art or for any stated purpose.

Art Unit: 2185

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyer et al. (US PAT. 5,410,546 hereinafter Boyer) in view of Lo et al. (US PAT. 6,324,178 hereinafter Lo).

Regarding claim 9, Boyer differs from the claimed invention in not specifically teaching data bus being designated according to the IEEE 1394 standard and the apparatus is part of data link layer module in the interface for this data bus. However, Lo teaches IEEE 1394 serial bus communication standard becoming a popular standard adopted by manufacturers of computer systems and peripheral components for its high speed and interconnection flexibilities (col. 1 lines 31-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Boyer in having data bus being designated according to the IEEE 1394 standard and the apparatus is part of data link layer module in the interface for this data bus, as per teaching of Lo, because it provides high speed and interconnection flexibilities.

Response to Arguments

6. Applicant's arguments filed 3/27/2006 have been fully considered but they are not persuasive.

In response to applicant's argument that Boyer fails to disclose the payload data field being divided into **data blocks having a defined length**, a combination of **a defined number n of data block forming a data source packet** of fixed length, it is noted that Boyer clearly teaches and a data portion, read as a payload data field, the data portion being divided into data blocks having a defined length, i.e., to write the variable length data packet into page buffers having a defined length, where each page buffer has equal size section (col. 20-24 and col. 10

Art Unit: 2185

lines 31-35), a combination of a defined number n of data blocks forming a data source packet of fixed length, i.e., combining a defined number of multiple page buffers forming a data packet of fixed length (col. 6 lines 26-40 and col. 10 lines 9-17). By given broadest reasonable interpretation of the claimed language, one skill in the art would recognize that the recited data blocks having a defined length does correspond to the page buffers taught by Boyer. Thus, Boyer discloses that the data in the data portion of the packet is divided into data blocks having a defined length.

In response to applicant's argument that Boyer fails to disclose modulo- n counting of data blocks, it is noted that Boyer clearly teaches a counter (415, figure 4) for carrying out a modulo- n counting of the data block in order to determine the data source packet boundaries (col. 13 lines 1-23). Note while the claimed language fail to clearly define the novelty of modulo- n counting. Thus, the counter of Boyer anticipates the modulo- n counting of data block as recited in the claimed language. Thus, Boyer discloses each and every limitation of the present claims 1-3 and 5-8. Furthermore, claims 4 and 9 remain rejecting under Boyer and the combination of Boyer and Lo, respectively.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Oda et al. (US PAT. 6,157,674) discloses a method of transmitting data via an asynchronous transfer mode communication line capable of simplifying and facilitating the calculation of the remaining capacity of STD buffers (col. 1 line 55 through col. 2 line 64).

Art Unit: 2185

Agarwal (US PAT. 6,931,009) discloses a method of assembling a plurality of frames including packet-formatted data according to a predetermined frame format for transmission in a communication signal in a wireless and satellite environment (abstract).

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

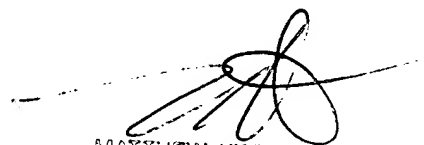
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is (571) 272-4183. The examiner can normally be reached on Tue-Fri 8:30 AM-6:00 PM, and alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2185

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li
Patent Examiner
Art Unit 2185



MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100